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TOWNSEND AND TOWNSEND AND CREW LLP / AMAT
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/362,504
Filing Date: July 27, 1999
Appellant(s): RAVI ET AL.

Chung-Pok Leung
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 30, 2005 appealing from the Office action mailed April 28, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: Claim 16 stands rejected under 35 USC 102(b), or in the alternative, under 35 USC 103(a).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claim 16 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Jin Onuki et al

Claims 17-19, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boys et al (USPat.4,500,408) in view of Jin Onuki et al

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Shijian et al (USPat. 5,772,771 A) in view of Jin Onuki et al

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Shijian et al (USPat. 5,77,2771 A) and Jin Onuki et al in view of Boys et al (USPat.4,500,408)

Claims 23, 24, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin Onuki et al in view of Matsura (USPat. 5,319,247)

Claim 25-30, 33, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boys et al (USPat.4,500,408) and Jin Onuki et al[1] in view of Li, Shijian et al (USPat. 5,772,771 A)

(10) Response to Argument

The sum-total of Applicant's arguments are centered on the Examiner's primary base reference to Jin Onuki et al. As cited in the Examiner's final rejection, Onuki's section 2, Figures 1(a) and 1(b) appear to either anticipate or make obvious Applicant's claimed inventions. Independent method claim 16 and independent apparatus claims 17, 20, and 32 all require steps taken, either by a controller/computer or in method form, that a first film(s) be deposited on a substrate by

[1] High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s*, Vol. 266 (1995), pp. 182-188.

first applying sputtering energy and not biasing the substrate followed by maintaining sputtering energy and also biasing the substrate to deposit additional film(s).

Page 8 of the brief states:

"

Onuki et al, however, specifically discloses terminating the sputtering power during application of the bias voltage....

"

With regard to Onuki's Figure 1(a) and 1(b), the Examiner cited in the final rejection that "It is not clear in Jin Onuki's Figure 1a and accompanying text that Onuki's conventional sputtering is one complete process, distinct processes, or is a process applied recursively. However, Jin Onuki's disclosure, taken as a whole, teaches that it would have been obvious to one of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b."

Onuki's Figure 1(a) teaches a "Conventional Sputtering" procedure. Onuki's Figure 1(a) has two boxes that appear to a "Conventional DC Sputtering" application and "Conventional DC Bias Sputtering" application. At first appearance, Onuki's Figure 1(a) appears to teach distinct processes, however, Onuki's Figure 1(b), immediately below Figure 1(a), shows, and the discussion supports (Section 2.1) one complete process where each box represents a processing *state that is repeated* over several times to deposit films discussed in section 2.1. Each of the boxes in Figure 1(b) switches sputtering on and off out of phase with a bias voltage. The Examiner thus believes that there is sufficient teaching in Onuki's Figure 1(a),(b) to suggest that Onuki's disclosure, taken as a whole, teaches that it would have been obvious to one of ordinary

skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b. Clearly, Figure 1(a) can, at a glance, be quickly interpreted as a continuous process thus anticipating Applicant's invention, or at least, upon further reading of Onuki, be a process that can be conducted recursively (as suggested by Figure 1(b)) again meeting applicant's claimed invention as conveyed in the Examiner's final action.

Applicant further states on page 8:

"

Onuki et al clearly does not teach depositing two different layers.

"

With respect to independent method claim 16 and independent apparatus claims 17, 20, and 32 that the reference fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "Onuki et al clearly does not teach depositing two different layers.") is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Independent claims 16, 17, 20, and 32 do not distinguish on film identity in the distinct processing steps. In fact, independent claims 17, 20, and 32 are broad enough to read on a single film identity being deposited under different processing conditions. Claims 16, 17, 20, and 32 each only require a "first layer" and "second layer". Independent article claim 23 is rejected separately and does require film identities – "metal layer" and "insulating layer". Yet, with respect to claim 23, the Examiner cites Onuki as teaching at least one metal layer (Al; Figure 4) formed above said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1); and at least one insulating layer (SiO2; Figure 4)

formed between said metal layer (Al; Figure 4) and said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1).

Applicant states, with respect to claim 23:

"

Nor does Jin Onuki et al recognize that the first layer formed without biasing the plasma is a reduced stress layer for reducing the stress of films deposited on the substrate.

" (page 8, bottom)

and

"

...Onuki et al does not teach or suggest two silicon oxide layers, wherein the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer.

" (page 14, top)

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In particular, the Examiner cites Matsura as teaching a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Operating conditions of pressure: 1mTorr<=100mT<=10Torr (column 6, line 33) and temperature: 100°C <= 350°C <= 450°C <= 500°C (column 6, line 38) are specifically met by Matsuura.

With respect to claim 18, Applicant states:

“

In addition, claim 18 further recites that the program includes instructions for depositing a plurality of the first layers and second layers until the desired thickness of the film is reached. The references do not disclose or suggest depositing a plurality of first layers by sputtering without biasing the plasma and second layers by sputtering and biasing the plasma.

“

Claims 17-19, 31, and 32 were rejected under Boys et al (USPat.4,500,408) in view of Jin Onuki et al. Each reference is directed to sputtering methods. In particular, Boys teaches a memory (column 8, lines 54-69) coupled to Boy's controller (57,58; Figure 1; column 8, lines 43-54) and storing a program (column 8, lines 54-69) for directing the operation of Boy's system, Boy's program (column 8, lines 54-69) including a set of instructions for depositing a film by first, controlling Boy's gas distribution system (31-34; Figure 1; column 8, lines 5-40) to... (see Final rejection).

Because of the Examiner's citation of Boys et al as teaching Applicant's claimed elements, the Examiner does not understand Applicant's position of "The Examiner recognizes that Boys et al does not teach a controller or a memory storing a program" (Page 11 of brief). The Examiner's final rejection is clear to the contrary.

Applicant states, with respect to claim 23:

“

...the Examiner alleges that "the sole difference between the claimed invention and the above conveyed prior art is the lack of intended use in Applicant's product claim."

“

The Examiner has not made this argument as part of his rejection of claims 23, 24, and 36. What the Examiner was intending to point out in the response to arguments section of the final rejection is that because Matsura teaches the same materials, then because the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent (In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977); MPEP 2112.01). The Examiner further pointed out, in his rejection of claims 23, 24, and 36, that Matsura teaches a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1).

Applicant's state:

"

The claim features not taught or suggested in Onuki et al and Matsura are not merely intended use features.

"

In response, Applicants mis-state the Examiner's interpretation of apparatus features that the Examiner believes to be intended use. Nowhere in the rejection of article claims 23, 24, and 36 does the Examiner apply an intended use argument. See final rejection. Indeed *all elements* in article claims 23, 24, and 36 are fully accorded patentable weight. Only in Apparatus claims 17-22, and 25-31 does the Examiner apply intended use arguments directed to process gas and/or film identities. See the final rejection.

In response to applicant's argument (third paragraph, page 14) that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized

that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

With respect to Applicant's arguments with respect to claims 24 and 36, see last paragraph page 14, it was Jin Onuki was cited as teaching an integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23, further comprising: (d) a second metal layer ("Al"; Figure 4(3)) formed above said semiconductor substrate (20; Figure 1; column 3, lines 49-65) - claim 24. Onuki's integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23 wherein the first silicon oxide layer (SiO2; Figure 4) is deposited on the substrate (Figure 4; "Si wafers" , Section 2.1) by placing the substrate in a process chamber (inherent, "base pressure before sputtering was $2x10^{-7}$ Pa" Section 2.1) applying a sputtering power ("The sputtering power was 4 kW..., Section 2.1, Figure 1a) to reactants to generate a plasma in the process chamber - claim 36.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Rudy Zervigon

Primary Examiner, Art Unit 1763

2/21/6

Conferees:

Parviz Hassanzadeh, SPE Art Unit 1763 P.L.

Glenn Caldarola, SPE Art Unit 1764

Rudy Zervigon, Primary Examiner, Art Unit 1763

Glenn Caldarola
Supervisory Patent Examiner
Technology Center 1700

Caldarola
Examiner
1700